REMARKS

This Amendment responds to the Office Action mailed July 21, 2005 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1, 4-6, 30, 32-36, 39 and 41 were previously pending in the application. Claims 8-29 and 43-45 have been withdrawn from consideration. Claims 2-3, 7, 31, 37-38, 40 and 42 were previously cancelled. By this Amendment, claims 1, 6, 30, 36 and 41 are amended. Claims 34 and 35 are cancelled without prejudice or disclaimer. Accordingly, claims 1, 4-6, 30, 32-33, 36, 39 and 41 are pending for examination in the application. Claims 1, 6, 30, 36 and 41 are independent claims. No new matter has been added.

The Examiner has rejected claims 1, 6, 30, 34-36, 39 and 41 under 35 U.S.C. §102(e) as anticipated by Hanawa et al. (US 6,282,505). Claims 4-5 and 32-33 are rejected under 35 U.S.C. §103(a) as unpatentable over Hanawa et al. in view of Liao et al. (US 6,857,061). The rejections are respectfully traversed.

Hanawa discloses a multi-port memory subdivided into a plurality of memory banks, each of the memory banks including means for storing therein data and an address of the data (column 2, lines 47-50). An address from a first memory port is input to a first memory bank in a first cycle and a comparison is made to determine whether the data to be accessed is stored in the first memory bank. If the data is stored in the first memory bank, the data is accessed. If the data is missing, the address is input to a second memory bank in a second cycle and a comparison is made to determine whether the data to be accessed is stored in the second memory bank (column 3, lines 22-34). The two memory banks can be accessed simultaneously (column 3, lines 46-52), but different ways in the same memory bank cannot be accessed simultaneously.

Amended claim 1 is directed to a cache memory system and requires, in part, an associative cache including a plurality of memory locations for storing data and addresses associated with the data, the memory locations being organized as two or more ways and each address presented to the

associative cache being compared with the addresses stored in each of the two or more ways, and at least one controller that enables a first device to access a first way selected from the two or more ways and enables a second device to access a second way selected from the two or more ways.

Hanawa does not disclose or suggest a cache memory system including an associative cache in which a first device can access a first way selected from two or more ways and a second device can access a second way from the two or more ways, such that the first and second ways can be accessed concurrently by the first and second devices, respectively, as claimed. Hanawa, by contrast, discloses a cache memory that is effectively divided into two separate associative caches in two memory banks. An address input to the Hanawa cache memory is supplied to only one of the associative caches at any given time. If the address to be accessed is not stored in the first associative cache, the address is provided to the second associative cache in a second cycle. Thus, Hanawa does not disclose a cache memory system wherein first and second ways of an associative cache can be accessed concurrently by first and second devices, as required by Applicants' claim 1. For these reasons, amended claim 1 is clearly and patentably distinguished over Hanawa, and withdrawal of the rejection is respectfully requested. Claims 4 and 5 depend from claim 1 and are patentable over Hanawa for at least the same reasons.

Amended claim 6 is directed to a cache memory system and requires, in part, an associative cache including a plurality of memory locations to store data and addresses associated with the data, the memory locations being organized as two or more ways and each address presented to the associative cache being compared with the addresses stored in each of the two or more ways, a plurality of cache outputs for providing data retrieved from the memory locations, and first and second multiplexers having multiplexer inputs coupled to at least some of the memory locations and multiplexer outputs coupled to the plurality of cache outputs to enable the first multiplexer to select data from a first way and to enable the second multiplexer to select data from a second way, the selected data from the first and second ways being provided concurrently on respective ones of the plurality of cache outputs.

As discussed above, Hanawa does not disclose or suggest a cache memory system wherein data from first and second ways of an associative cache can be provided concurrently on the cache outputs, as claimed. Instead, Hanawa discloses a cache memory that is effectively divided into two separate associative caches in two memory banks, and accessing the separate associative caches concurrently. Accordingly, Hanawa does not disclose or suggest the cache memory system of amended claim 6, and withdrawal of rejection is respectfully requested.

Amended claim 30 is directed to a method of operating an associative cache having a plurality of memory locations for storing data and addresses associated with the data, the memory locations being organized as two or more ways. The method comprises accessing with a first device a first way selected from the two or more ways and accessing with a second device a second way selected from the two or more ways. Accessing includes comparing each address presented to the associative cache with the addresses stored in each of the two or more ways. The first and the second ways can be accessed concurrently by the first and second devices, respectively.

As discussed above in connection with claims 1 and 6, Hanawa does not disclose a method of operating an associative cache wherein first and second ways of an associative cache can be accessed concurrently by first and second devices, respectively. Instead, Hanawa discloses a cache memory that is effectively divided into two separate associative caches in two memory banks, and accessing the separate associative caches concurrently. For these reasons and for the reasons discussed above in connection with claims 1 and 6, amended claim 30 is clearly and patentably distinguished over Hanawa. Accordingly, withdrawal of the rejection is respectfully requested. Claims 32 and 33 depend from claim 30 and are patentable over Hanawa for at least the same reasons.

Claim 36 is directed to a method of operating an associative cache having a plurality of memory locations for storing data and addresses associated with the data, the memory locations being organized as two or more ways. The method comprises using multiple decoders to decode respective addresses provided to the cache including using a first decoder to decode a first address to access a first way and using a second decoder to decode a second address to access a second way.

Each address presented to the associative cache is compared with the addresses stored in each of the two or more ways. The first and second ways can be accessed concurrently by the first and second addresses, respectively.

Hanawa does not disclose or suggest a method of operating an associative cache as defined by amended claim 36. In particular, Hanawa does not disclose or suggest using first and second decoders to decode addresses supplied to an associative cache such that the first and second ways of the associative cache can be accessed concurrently by first and second addresses, respectively. Instead, Hanawa discloses a cache memory that is effectively divided into two separate associative caches in two memory banks, and accessing the separate associative caches concurrently. For these reasons and the reasons discussed above in connection with claims 1, 6 and 30, claim 36 is clearly and patentably distinguished over Hanawa. Claim 39 depends from claim 36 and is patentable over Hanawa for at least the same reasons. Accordingly, withdrawal of the rejection is respectfully requested.

Claim 41 is directed to a cache memory system and contains limitations that parallel the limitations of claim 1. Amended claim 41 is clearly patentable over Hanawa for at least the reasons discussed above in connection with claim 1.

Based upon the above discussion, claims 1, 4-6, 30, 32-33, 36, 39 and 41 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee

occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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